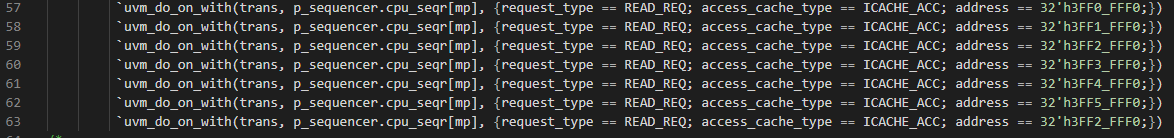
1. **Failing Test name**

Icache read Miss with no free block available

1. **Test description (Describe the planned scenario and the expected result)**

L1 Instruction cache read miss with Free block is unavailable: LRU Replacement is required.

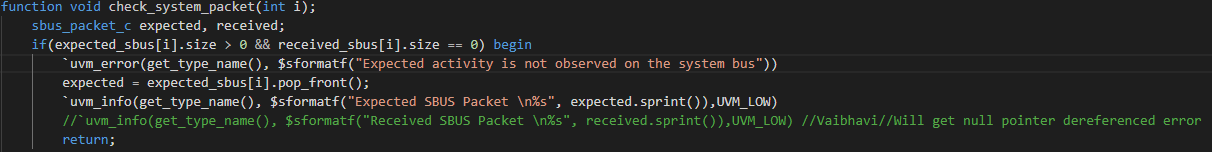
Targeted test to verify LRU bug:



Line 63 read at 32’h3FF2\_FFF0 should be read miss should be serviced by L2, instead was serviced by L1 cache as seen in error message and waveform.

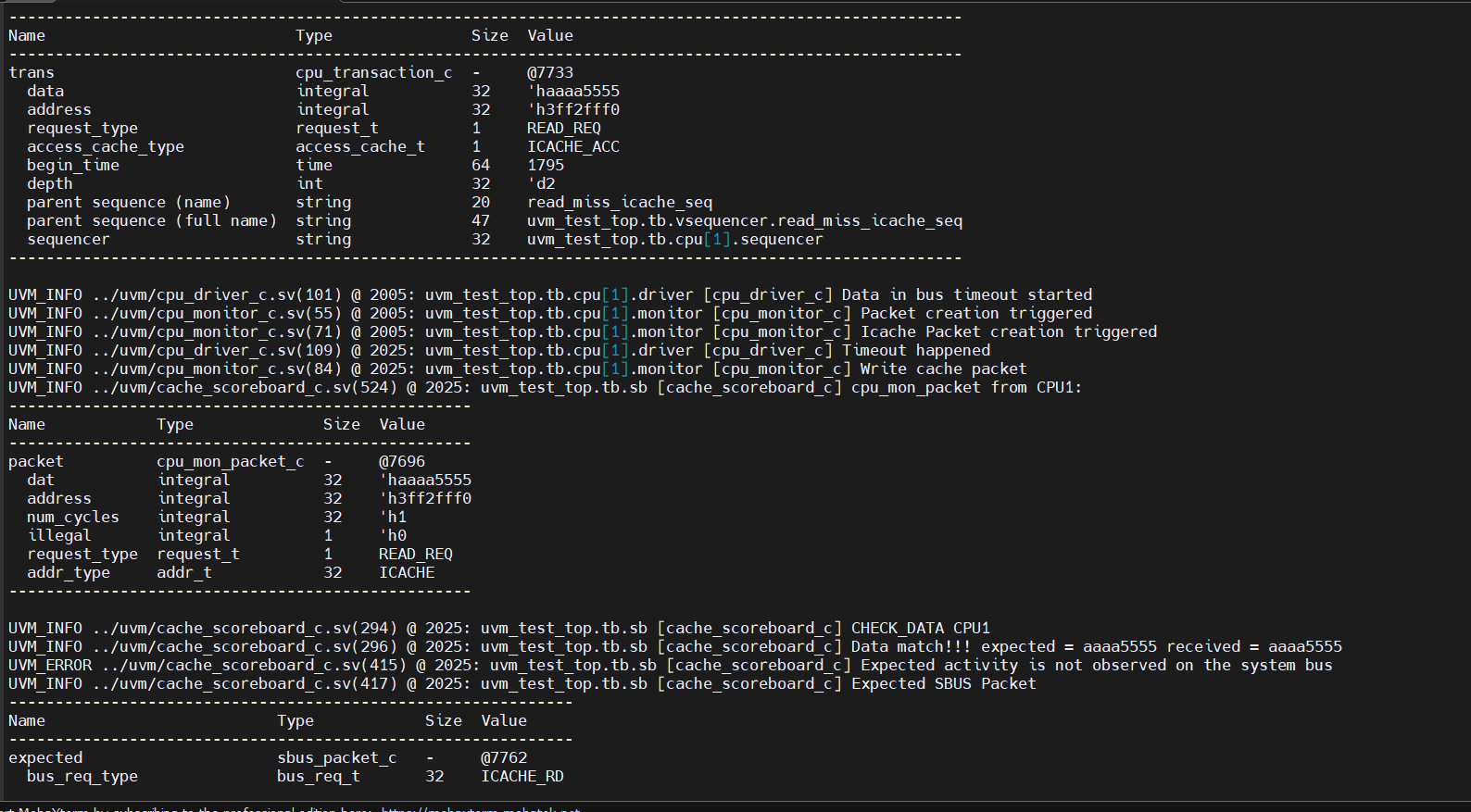
1. **Failing assertion that helped you identify the bug**

Scoreboard does not receive packets from Sbus and throws error.

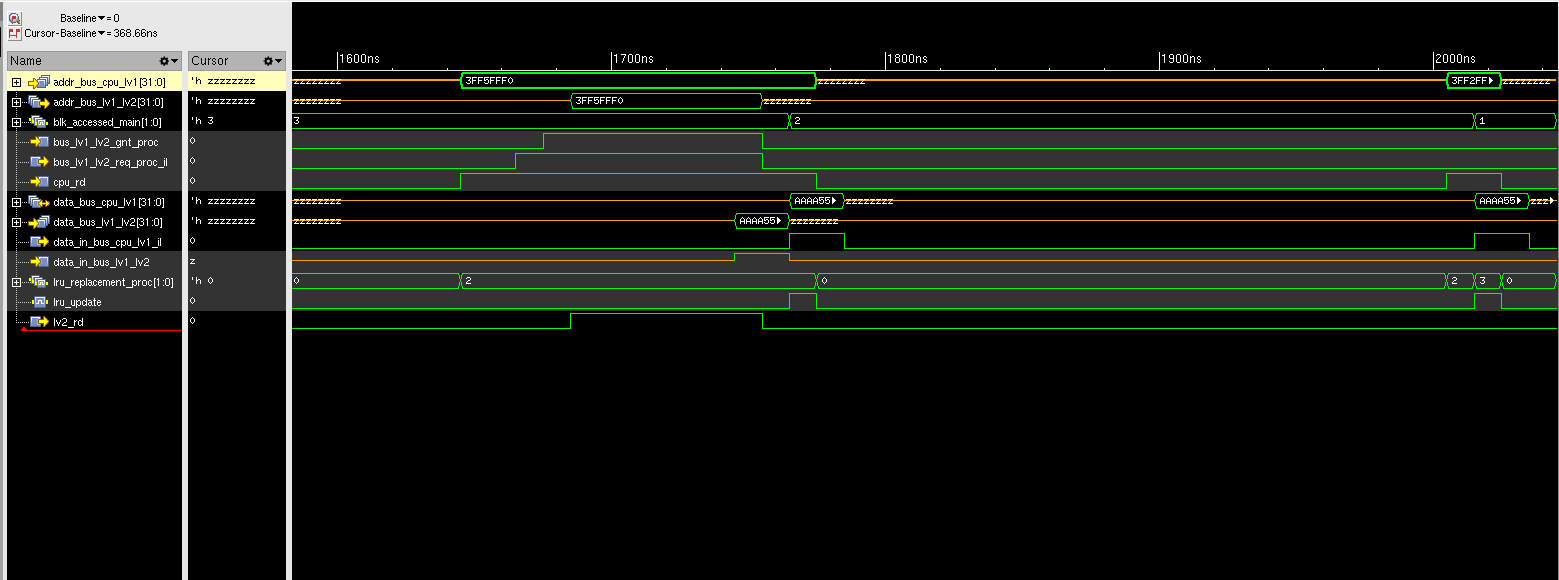


1. **Debug Process**

Error message:



Block serviced by LV1 instead of LV2. This means the block should have been replaced but was not replaced.



Bus\_lv1\_lv2\_req\_proc did not assert high.

1. **Erroneous RTL file name**

lru\_block\_lv1.sv

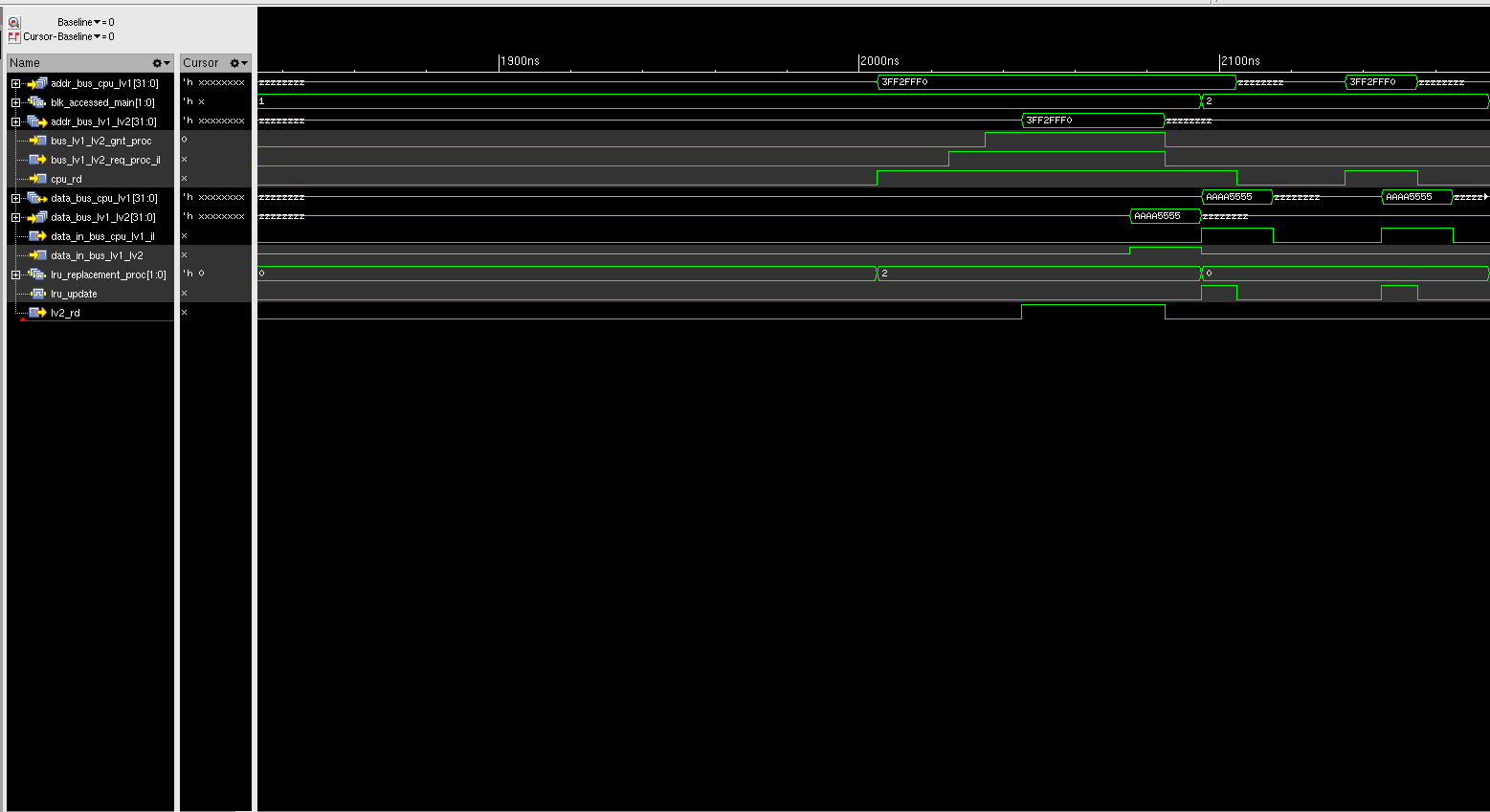
1. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**



1. **Corrected RTL code (only mention the corrections)**

****

1. **Waveform after fix:**

****

Read request being serviced by L2 as block was replaced.